In re Patent Application of
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Serial No. **NOT YET ASSIGNED**
Filed: **HEREWITH**

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Listing of the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-7 (canceled).

8. (new) A data storage device comprising:

a plurality of registers that can be addressed by address words;

p output ports; and

connecting means for connecting the plurality of registers to the p output ports in response to address words of p registers selected to read contents of the registers on the p ports respectively;

wherein all address words contain a specific bit and remaining bits, the registers are connected in pairs on each output port, each pair of registers including two registers with address words that only differ in a value of the specific bit, and for each pair of registers and for each output port, the connecting means comprise a pair of first switching means controlled in a complementary manner by the specific bit in the address word of one of the two registers, and a second switching means connected to the corresponding output port and controlled from the remaining bits of the address words of the two registers, the pair of first switching means being connected between the corresponding two registers and between the corresponding second switching means.

9. (new) A device according to Claim 8, wherein the registers comprise m memory points to store data with m bits; wherein one of the pair of first switching means associated with a register comprises m first elementary path gates connected to the corresponding m memory points in the register, the other of the pair of first switching means associated with the other register comprises m other first elementary path gates connected to the corresponding m memory points of the other register, a first elementary path gate connected to a memory point of the register being controlled in a complementary manner with respect to the other first elementary path gate connected to the corresponding memory point of the other register; and the second switching means comprises m second elementary path gates connected between the corresponding output port and m pairs formed from the first elementary path gates and the other first elementary path gates, respectively.

10. (new) A device according to Claim 9, further comprising:

a first elementary inverter connected between each memory point of a register and the p first elementary path gates associated with the register; and

a second elementary inverter connected between each second elementary path gate connected to an output port and the pair formed by the first elementary path gate and the other first elementary path gate associated with the other register in the pair of registers.

11. (new) A device according to Claim 9, wherein each first elementary path gate, and each other first elementary path gate comprise pairs of complementary MOS transistors, the control gates of two opposite types of transistors belonging respectively to the two pairs being connected together to enable complementary control of the first elementary path gate and of the other first elementary path gate.

12. (new) A device according to Claim 8, wherein the first switching means associated with the two registers in a pair are located relatively close to each other.

13. (new) A device according to Claim 8, wherein the registers, output ports and connecting means define an integrated circuit.

14. (new) A device according to Claim 8, further comprising:

a controller to generate the address words; and

a digital signal processor (DSP) to control the controller in a read mode.

15. (new) A data storage device comprising:

a plurality of registers with addresses having a specific bit and remaining bits;

p output ports, the registers being connected in pairs on each output port, each pair of registers including

two registers having addresses that only differ in a value of the specific bit; and

connections to connect the plurality of registers to the p output ports in response to addresses of p registers selected to read contents of the registers on the p output ports respectively;

for each pair of registers and for each output port, the connections comprise a pair of first complementary controlled switches controlled by the specific bit in the addresses of one of the pair of registers, and a second switch connected to the corresponding output port and controlled by the remaining bits of the addresses of the pair of registers, the pair of first complementary controlled switches being connected between the corresponding pair of registers, and between the corresponding pair of registers and the corresponding second switch.

16. (new) A device according to Claim 15, wherein the registers comprise m memory points to store data with m bits; wherein one of the pair of first switches associated with a register comprises m first elementary path gates connected to the corresponding m memory points in the register, the other of the pair of first switches associated with the other register comprises m other first elementary path gates connected to the corresponding m memory points of the other register, a first elementary path gate connected to a memory point of the register being controlled in a complementary manner with respect to the other first elementary path gate connected to the corresponding memory

point of the other register; and the second switch comprises m second elementary path gates connected between the corresponding output port and m pairs formed from the first elementary path gates and the other first elementary path gates, respectively.

17. (new) A device according to Claim 16, further comprising:

a first elementary inverter connected between each memory point of a register and the p first elementary path gates associated with the register; and

a second elementary inverter connected between each second elementary path gate connected to an output port and the pair formed by the first elementary path gate and the other first elementary path gate associated with the other register in the pair of registers.

18. (new) A device according to Claim 17, wherein each first elementary path gate, and each other first elementary path gate comprise pairs of complementary MOS transistors, the control gates of two opposite types of transistors belonging respectively to the two pairs being connected together for complementary control of the first elementary path gate and of the other first elementary path gate.

19. (new) A device according to Claim 15, wherein the first switches associated with the two registers in a pair are located relatively close to each other.

20. (new) A device according to Claim 15, wherein the registers, output ports and connections define an integrated circuit.

21. (new) A device according to Claim 15, further comprising:

a controller to generate the addresses; and

a digital signal processor (DSP) to control the controller in a read mode.

22. (new) A method of reading data in a data storage device comprising:

providing a plurality of registers with addresses having a specific bit and remaining bits;

providing p output ports, the registers being connected in pairs on each output port, each pair of registers including two registers having addresses that only differ in a value of the specific bit; and

providing connections to connect the plurality of registers to the p output ports in response to addresses of p registers selected to read contents of the registers on the p output ports respectively;

for each pair of registers and for each output port, the connections comprise a pair of first complementary controlled switches controlled by the specific bit in the addresses of one of the pair of registers, and a second switch connected to the corresponding output port and controlled by the remaining bits of the addresses of the pair of registers,

the pair of first complementary controlled switches being connected between the corresponding pair of registers, and between the corresponding pair of registers and the corresponding second switch.

23. (new) A method according to Claim 22, wherein the registers comprise m memory points to store data with m bits; wherein one of the pair of first switches associated with a register comprises m first elementary path gates connected to the corresponding m memory points in the register, the other of the pair of first switches associated with the other register comprises m other first elementary path gates connected to the corresponding m memory points of the other register, a first elementary path gate connected to a memory point of the register being controlled in a complementary manner with respect to the other first elementary path gate connected to the corresponding memory point of the other register; and the second switch comprises m second elementary path gates connected between the corresponding output port and m pairs formed from the first elementary path gates and the other first elementary path gates, respectively.

24. (new) A method according to Claim 23, further comprising:

connecting a first elementary inverter between each memory point of a register and the p first elementary path gates associated with the register; and

connecting a second elementary inverter between each second elementary path gate connected to an output port and the pair formed by the first elementary path gate and the other first elementary path gate associated with the other register in the pair of registers.

25. (new) A method according to Claim 24, wherein each first elementary path gate, and each other first elementary path gate comprise pairs of complementary MOS transistors, the control gates of two opposite types of transistors belonging respectively to the two pairs being connected together for complementary control of the first elementary path gate and of the other first elementary path gate.

26. (new) A method according to Claim 22, further comprising:

generating the addresses with a controller; and

controlling the controller in a read mode with a digital signal processor (DSP).